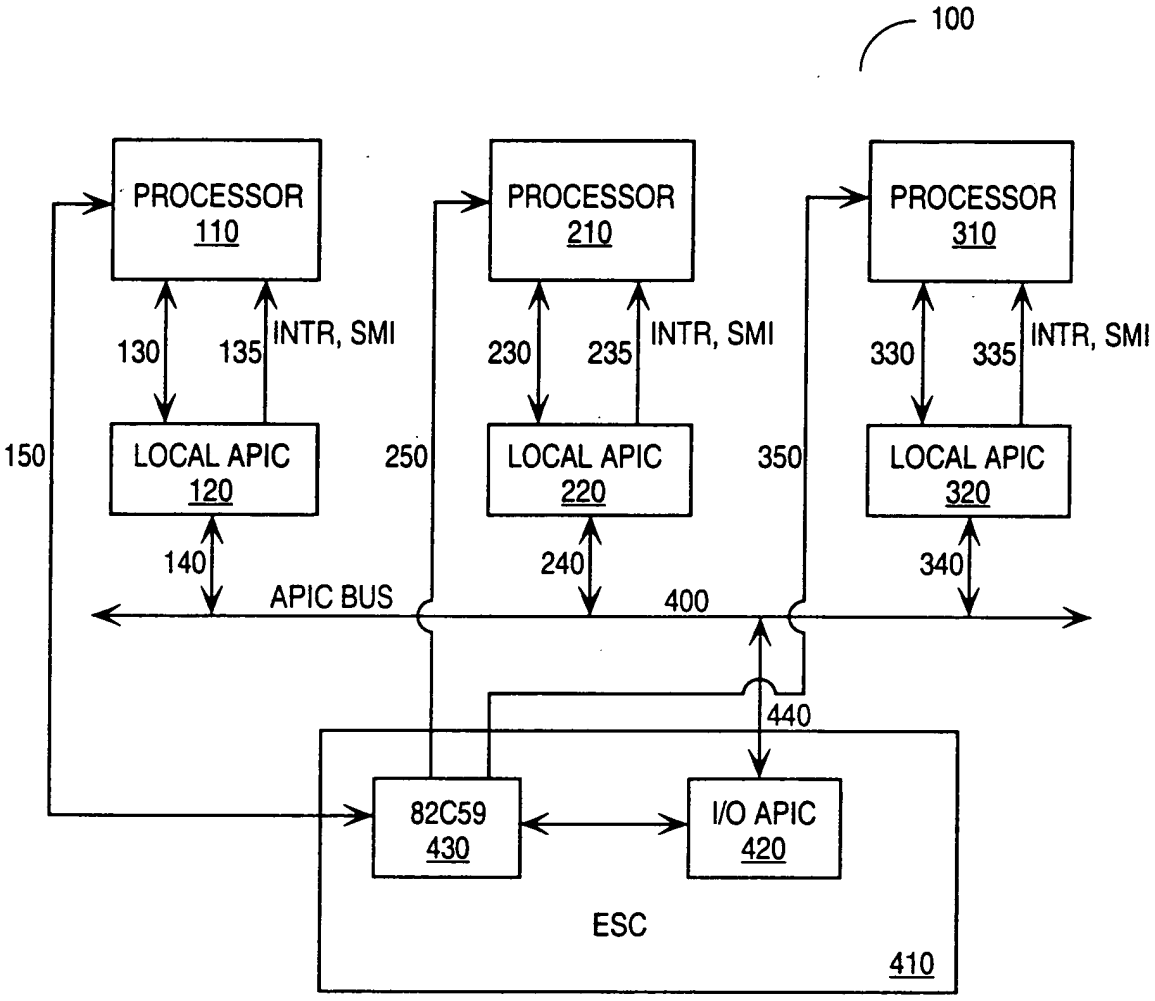
100
PROCESSOR
110
PROCESSOR
210
PROCESSOR
310
130
135
INTR, SMI
230
235
INTR, SMI
330
335
INTR, SMI
150
LOCAL APIC
120
250
LOCAL APIC
220
350
LOCAL APIC
320
140
240
340
APIC BUS
400
440
82C59
430
I/O APIC
420
ESC
410

FIG. 1

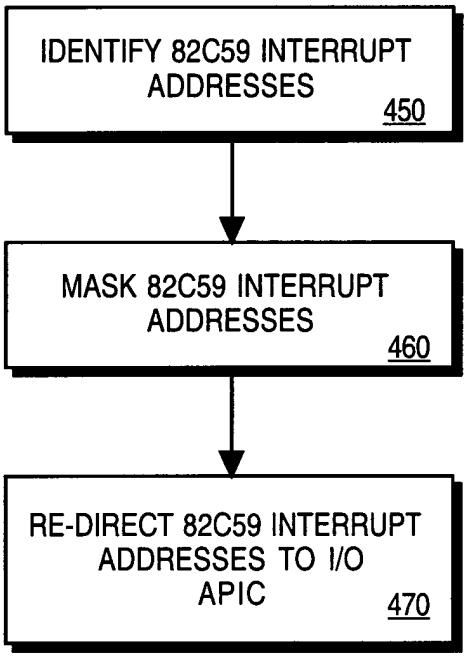
IDENTIFY 82C59 INTERRUPT ADDRESSES
450
MASK 82C59 INTERRUPT ADDRESSES
460
RE-DIRECT 82C59 INTERRUPT ADDRESSES TO I/O APIC
470

FIG. 2

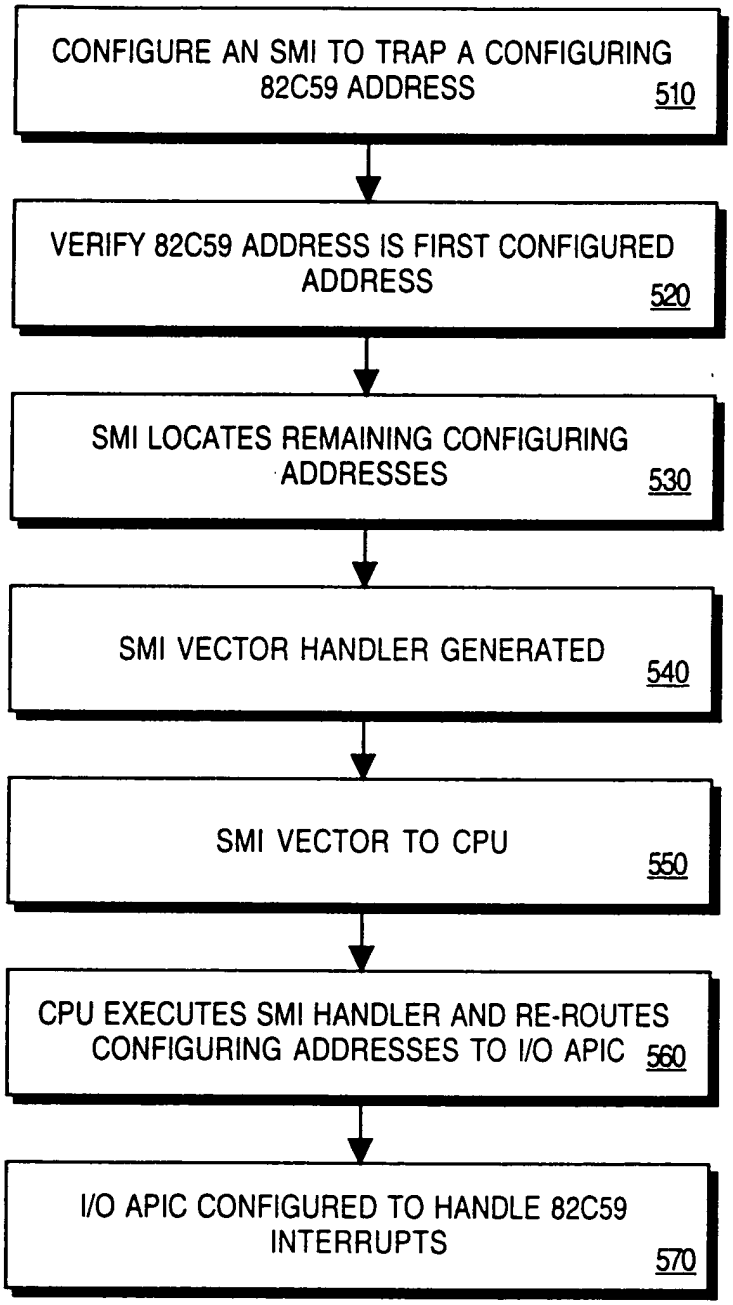
CONFIGURE AN SMI TO TRAP A CONFIGURING 82C59 ADDRESS 510
VERIFY 82C59 ADDRESS IS FIRST CONFIGURED ADDRESS 520
SMI LOCATES REMAINING CONFIGURING ADDRESSES 530
SMI VECTOR HANDLER GENERATED 540
SMI VECTOR TO CPU 550
CPU EXECUTES SMI HANDLER AND RE-ROUTES CONFIGURING ADDRESSES TO I/O APIC 560
I/O APIC CONFIGURED TO HANDLE 82C59 INTERRUPTS 570

FIG. 3